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WHAT IS CLAIMED IS:

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1. A calibration circuit, comprising:
a first component;
a digitally tunable second component;
a current source coupled to the first component to generate a first parameter of the first component, and coupled to the second component to generate a second parameter of the second component; and
10 a logic control block to digitally tune the second component as a function of the first and second parameters.

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2. The calibration circuit of claim 1 wherein the current source provides a first current to the first component and a second current to the second component.

3. The calibration circuit of claim 2 wherein the first current is substantially equal to the second current.

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4. The calibration circuit of claim 1 wherein the current source comprises a current mirror having a first output coupled to the first component and a second output coupled to the second component.

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5. The calibration circuit of claim 1 wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage.

6. The calibration circuit of claim 5 wherein the logic control block comprises a comparator to compare the first and second voltages, and control logic to digitally tune the second component as a function of the voltage comparison.

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7. The calibration circuit of claim 1 wherein the first component comprises a resistor.

8. The calibration circuit of claim 7 wherein the second component comprises a second resistor.

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9. The calibration circuit of claim 8 wherein the second resistor comprises a tunable resistor array.

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10. The calibration circuit of claim 9 wherein the tunable resistor array comprises a plurality of resistors coupled in series, and a plurality of switches each being coupled across a different one of said plurality of resistors.

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11. The calibration circuit of claim 10 wherein the logic control block generates a plurality digital bits as function of the first and second parameters, the digital bits each controlling a different one of the switches.

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12. The calibration circuit of claim 7 wherein the second component comprises a capacitor.

13. The calibration circuit of claim 12 wherein the capacitor comprises a tunable capacitor array.

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14. The calibration circuit of claim 13 wherein the tunable capacitor array comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of the capacitors.

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15. The calibration circuit of claim 14 wherein the logic control block generates a plurality digital bits as function of the first and second parameters, the digital bits each controlling a different one of the switches.

16. The calibration circuit of claim 12 further comprising a first switch coupled between the current source and the capacitor, and a second switch shunting the capacitor.

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17. The calibration circuit of claim 16 wherein the logic control block controls the first and second switches.

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18. A calibration circuit, comprising:
a first component;
a digitally tunable second component;

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generating means for generating a first parameter of the first component, and a second parameter of the second component; and

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tuning means for digitally tuning the second component as a function of the first and second parameters.

19. The calibration circuit of claim 18 wherein the generating means comprises a current source.

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20. The calibration circuit of claim 19 wherein the current source provides a first current to the first component and a second current to the second component.

21. The calibration circuit of claim 20 wherein the first current is substantially equal to the second current.

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22. The calibration circuit of claim 19 wherein the current source comprises a current mirror having a first output coupled to the first component and a second output coupled to the second component.

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23. The calibration circuit of claim 18 wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage.

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24. The calibration circuit of claim 23 wherein the tuning means comprises a comparator to compare the first and second voltages, and control logic to digitally tune the second component as a function of the voltage comparison.

25. The calibration circuit of claim 18 wherein the first component comprises a resistor.

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26. The calibration circuit of claim 25 wherein the second component comprises a second resistor.

27. The calibration circuit of claim 26 wherein the second resistor comprises a tunable resistor array.

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28. The calibration circuit of claim 27 wherein the tunable resistor array comprises a plurality of resistors coupled in series, and bypass means for bypassing at least one of said plurality of resistors.

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29. The calibration circuit of claim 28 the bypass means comprises a plurality of switches each being coupled across a different one of said plurality of resistors.

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30. The calibration circuit of claim 29 wherein the tuning means comprises means for generating a plurality digital bits as function of the first and second parameters, the digital bits each controlling a different one of the switches.

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31. The calibration circuit of claim 25 wherein the second component comprises a capacitor.

32. The calibration circuit of claim 31 wherein the capacitor comprises a tunable capacitor array.

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33. The calibration circuit of claim 32 wherein the tunable capacitor array comprises a plurality of capacitors coupled in parallel, and switching means for switching at least one capacitor in and out of the tunable capacitor array.

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34. The calibration circuit of claim 33 wherein the switching means comprises a plurality of switches each being coupled in series to a different one of the capacitors.

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35. The calibration circuit of claim 34 wherein the tuning means generates a plurality digital bits as function of the first and second parameters, the digital bits each controlling a different one of the switches.

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36. The calibration circuit of claim 31 wherein the generating means comprises a current source, the calibration circuit further comprising a first switch coupled between the current source and the capacitor, and a second switch shunting the capacitor.

37. The calibration circuit of claim 36 wherein the tuning means controls the first and second switches.

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38. A calibration circuit, comprising:
a current source;
a first component coupled to the current source through a first node;
5 a digitally tunable second component coupled to the current source through a second
node;
a comparator having an input coupled to the first and second nodes, and an output; and
control logic coupled between the output of the comparator and the second
component.

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39. The calibration circuit of claim 38 wherein the current source provides a first current
to the first component and a second current to the second component, the first and second currents
being substantially equal.

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40. The calibration circuit of claim 38 wherein the current source comprises a current
mirror having a first output coupled to the first component and a second output coupled to the second
component.

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41. The calibration circuit of claim 38 wherein the first component comprises a resistor.

42. The calibration circuit of claim 41 wherein the second component comprises a second
resistor.

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43. The calibration circuit of claim 42 wherein the second resistor comprises a tunable
resistor array.

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44. The calibration circuit of claim 43 wherein the tunable resistor array comprises a
plurality of resistors coupled in series, and a plurality of switches each being coupled across a different
one of said plurality of resistors.

45. The calibration circuit of claim 41 wherein the second component comprises a
capacitor.

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46. The calibration circuit of claim 45 wherein the capacitor comprises a tunable capacitor
array.

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47. The calibration circuit of claim 46 wherein the tunable capacitor array comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of the capacitors.

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48. The calibration circuit of claim 45 further comprising a first switch coupled between the current source and the capacitor, and a second switch shunting the capacitor.

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49. The calibration circuit of claim 48 wherein the control logic is coupled to the first and second switches.

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50. A transceiver, comprising:
a calibration circuit comprising a first component, a digitally tunable second component, a current source coupled to the first component to generate a first parameter of the first component and coupled to the second component to generate a second parameter of the second component, and a logic control block having a control output to digitally tune the second component as a function of the first and second parameters; and
a digitally tunable transceiver component tuned by the control output of the logic control block.

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51. The transceiver of claim 50 wherein the current source provides a first current to the first component and a second current to the second component.

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52. The transceiver of claim 51 wherein the first current is substantially equal to the second current.

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53. The transceiver of claim 50 wherein the current source comprises a current mirror having a first output coupled to the first component and a second output coupled to the second component.

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54. The transceiver of claim 50 wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage.

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55. The transceiver of claim 54 wherein the logic control block comprises a comparator to compare the first and second voltages, and control logic comprising the control output to digitally tune the second component as a function of the voltage comparison.

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56. The transceiver of claim 50 wherein the first component comprises a resistor.

57. The transceiver of claim 56 wherein the second component comprises a second resistor.

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58. The transceiver of claim 57 wherein the second resistor comprises a tunable resistor array.

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59. The transceiver of claim 58 wherein the tunable resistor array comprises a plurality of resistors coupled in series, and a plurality of switches each being coupled across a different one of said plurality of resistors.

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60. The transceiver of claim 59 wherein the logic control block generates a plurality digital bits as function of the first and second parameters, the control output of the logic control, block comprising the digital bits, the digital bits each controlling a different one of the switches.

61. The transceiver of claim 60 wherein the transceiver component comprises a transceiver resistor.

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62. The transceiver of claim 61 wherein the transceiver resistor comprises a transceiver tunable resistor array.

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63. The transceiver of claim 62 wherein the transceiver tunable resistor array comprises a plurality of transceiver resistors coupled in series, and a plurality of transceiver switches each being coupled across a different one of said plurality of transceiver resistors.

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64. The transceiver of claim 63 wherein the digital bits generated by the logic control block each controls a different one of the transceiver switches.

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65. The transceiver of claim 56 wherein the second component comprises a capacitor.

66. The transceiver of claim 65 wherein the capacitor comprises a tunable capacitor array.

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67. The transceiver of claim 66 wherein the tunable capacitor array comprises a plurality of capacitors coupled in parallel, and a plurality of switches each being coupled in series to a different one of the capacitors.

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68. The transceiver of claim 67 wherein the logic control block generates a plurality digital bits as function of the first and second parameters, the control output of the logic control, block comprising the digital bits, the digital bits each controlling a different one of the switches.

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69. The transceiver of claim 68 wherein the transceiver component comprises a transceiver capacitor.

70. The transceiver of claim 69 wherein the transceiver capacitor comprises a transceiver tunable capacitor array.

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71. The transceiver of claim 70 wherein the transceiver tunable capacitor array comprises a plurality of transceiver capacitors coupled in parallel, and a plurality of transceiver switches each being coupled in series to a different one of the transceiver capacitors.

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72. The transceiver of claim 71 wherein the digital bits generated by the logic control block each controls a different one of the transceiver switches.

73. The transceiver of claim 65 further comprising a first switch coupled between the current source and the capacitor, and a second switch shunting the capacitor.

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74. The transceiver of claim 73 wherein the logic control block controls the first and second switches.

75. A transceiver, comprising:

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a calibration circuit comprising a first component, a digitally tunable second component, a current source coupled to the first component to generate a first parameter of the first

1 component and coupled to the second component to generate a second parameter of the second component, and a logic control block having a control output to digitally tune the second component as a function of the first and second parameters; and

5 a bandgap calibration circuit to generate a bandgap current substantially independent of temperature, the bandgap calibration circuit being responsive to the control output from the logic control block.

10 76. The transceiver of claim 75 wherein the current source provides a first current to the first component and a second current to the second component.

77. The transceiver of claim 76 wherein the first current is substantially equal to the second current.

15 78. The transceiver of claim 75 wherein the current source comprises a current mirror having a first output coupled to the first component and a second output coupled to the second component.

20 79. The transceiver of claim 75 wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage.

25 80. The transceiver of claim 79 wherein the logic control block comprises a comparator to compare the first and second voltages, and control logic comprising the control output to digitally tune the second component as a function of the voltage comparison.

81. The transceiver of claim 75 wherein the first component comprises a resistor.

30 82. The transceiver of claim 81 wherein the second component comprises a second resistor.

83. The transceiver of claim 82 wherein the second resistor comprises a tunable resistor array.

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84. The transceiver of claim 83 wherein the tunable resistor array comprises a plurality of resistors coupled in series, and a plurality of switches each being coupled across a different one of said plurality of resistors.

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85. The transceiver of claim 84 wherein the logic control block generates a plurality digital bits as function of the first and second parameters, the control output of the logic control, block comprising the digital bits, the digital bits each controlling a different one of the switches.

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86. The transceiver of claim 85 wherein the bandgap calibration circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the first and second bias circuits being responsive to the control output from the logic control block.

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87. The transceiver of claim 86 wherein the summer comprises a cascode current mirror.

88. A method of calibration, comprising:

providing a first current to a first component to generate a first parameter;

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providing a second current to a second component to generate a second parameter; and

digitally tuning the second component as a function of the first and second parameters.

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89. The method of claim 88 wherein the first current is substantially equal to the second current.

90. The method of claim 88 further comprising generating a reference current, and mirroring the first and second currents to the reference current.

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91. The method of claim 88 wherein the second component comprises a plurality of resistors coupled in series, and the digital tuning of the second component comprises selectively bypassing at least one of the resistors.

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92. The method of claim 88 wherein the second component comprises a plurality of capacitors coupled in a parallel array, and the digital tuning of the second component comprises selectively switching at least one of the capacitors in or out of the array.

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93. The method of claim 88 wherein the second component comprises a capacitor, the method further comprising charging the capacitor before digitally tuning the second component and discharging the capacitor after the second component is digitally tuned.

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94. The method of claim 88 wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage.

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95. The method of claim 94 wherein the digital tuning of the second component comprises initially tuning the second component, comparing the first voltage to the second voltage generated across the initially tuned second component, and retuning the second component if the comparison of the first and second voltages do not match.

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96. The method of claim 95 wherein the initial tuning of the second component comprises initially tuning the second component with a digital word.

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97. The method of claim 96 wherein the retuning of the second component comprises incrementing the digital word, and retuning the second component with the incremented digital word.

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98. The method of claim 94 wherein the digital tuning of the second component comprises initially tuning the second component with a digital word, comparing the first voltage to the second voltage generated across the initially tuned second component, and latching the digital word if the comparison of the first and second voltages match.

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99. The method of claim 98 further comprising tuning a transceiver component with the latched digital word.

100. The method of claim 99 wherein the transceiver component comprises a plurality of resistors coupled in series, and the tuning of the transceiver component comprises selectively bypassing at least one of the resistors as a function of the latched digital word

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101. The method of claim 99 wherein the transceiver component comprises a plurality of capacitors coupled in a parallel array, and the tuning of the transceiver component comprises selectively switching at least one of the capacitors in or out of the array.

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102. The method of claim 98 further comprising calibrating a bandgap current with the latched digital word.

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103. The method of claim 102 wherein the calibration of the bandgap current comprises generating a first bias current exhibiting a positive temperature coefficient as a function of the latched digital word, generating a second bias current exhibiting a negative temperature coefficient as a function of the latched digital word, and summing the first and second bias currents.

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